1. An integrated circuit comprising:
a plurality of modules (M) processing applications, each having a local memory (LM);
a global memory (GM), which can be shared by said plurality of modules (M);
interconnected data communications paths, interconnecting said modules (M) and said global memory (GM); and
a memory managing unit (MMU) being associated with each of said modules (M), determines whether said local memory (LM) provides sufficient memory space for processing a currently processed application on one of the plurality of modules (M) and in response to determining that there is not sufficient memory space, issuing a reservation request for memory space within a global buffer (GB) in said global memory (GM) exclusively reserved for processing data of the one of the plurality of modules and in response to determining that there is not sufficient memory space, issuing a path request for a dedicated communication path between the one of the plurality of modules and the global buffer.

2. The integrated circuit according to claim 1, wherein said communication path having communication properties according to the path request.

3. The integrated circuit according to claim 1, further comprising a resource managing unit (RMU) allocating memory space in said global memory (GM) according to the reservation request of said memory managing unit (MMU).

4. The integrated circuit according to claim 3, wherein said resource managing unit (RMU) sets a communication path based on communication properties as required by said memory managing unit (MMU).

5. The integrated circuit according to claim 4, further comprising an address translation unit (ATU) associated with each of said modules (M) performing an address translation for data of an application, which data are stored in said global buffer (FB) in said global memory (GM).

6. The integrated circuit according to claim 3, wherein said resource managing unit (RMU) performs an access arbitration for said global memory (GM).

7. The integrated circuit according to claim 1, wherein said local memory (LM) comprises a prefetch buffer (PB) that prefetches data from said global buffer (FB).

8. A method for memory allocation in an integrated circuit comprising a plurality of modules (M) processing applications, wherein each module comprises a local memory (LM), a global memory (GM) shared between said plurality of modules (M), the method comprising:
determining whether said local memory (LM) provides sufficient memory space for processing a currently processed application of the one of the plurality of modules;
in response to determining that there is not sufficient memory space, issuing a reservation request for memory space within a global buffer (FB) in said global memory (GM) exclusively reserved for processing data of the one of the plurality of modules, in

response to the determining that there is not sufficient memory space, issuing a path request for a dedicated communication path between the one of the plurality of modules and the global buffer.

9. The integrated circuit of claim 3, wherein the RMU allocates memory space in said global memory in response to determining that there is adequate space in the global memory to support the reservation request and in response to determining that there is adequate transmission bandwidth to support the path request.

10. The integrated circuit of claim 1, wherein the MMU determines whether the LM provides sufficient memory space for the currently processed application by comparing the memory space in the LM to a predetermined value.

11. The integrated circuit of claim 3, wherein the RMU provides an address of the global buffer to the MMU and wherein the MMU uses the provided address to perform address translation between an address provided by the one of the plurality of modules to the address of the global buffer.